

MOSFET – P-Channel, QFET®

FQD3P50

-500 V, 4.9 Ω , -2.1 A

Description

This P-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- -2.1 A, -500 V, $R_{DS(on)} = 4.9 \Omega$ (Max.) @ $V_{GS} = -10$ V, $I_D = -1.05$ A
- Low Gate Charge (Typ. 18 nC)
- Low C_{rss} (Typ. 9.5 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_C = 20^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	-500	V
I_D	Drain Current		A
	- Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	-2.1 -1.33	
I_{DM}	Drain Current - Pulsed (Note 1)	-8.4	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	250	mJ
I_{AR}	Avalanche Current (Note 1)	-2.1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
P_D	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
	Power Dissipation ($T_A = 25^\circ\text{C}$) (Note 4)	2.5	W
T_J, T_{STG}	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	50 0.4	W W/ $^\circ\text{C}$
	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

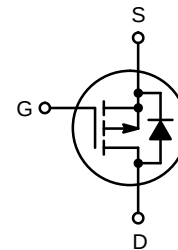
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $L = 102$ mH, $I_{AS} = -2.1$ A, $V_{DD} = -50$ V, $R_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq -2.7$ A, $di/dt \leq 200$ A/ms, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.
4. When mounted on the minimum pad size recommended (PCB Mount).

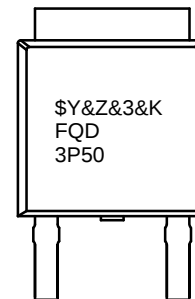


ON Semiconductor®

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MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Code
&3 = Date Code (Year and Week)
&K = Lot Code
FQD3P50 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FQD3P50	DPAK3 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FQD3P50

THERMAL CHARACTERISTICS

Symbol	Parameter	FQD3P50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. (Note 5)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W

5. When mounted on the minimum pad size recommended (PCB Mount).

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ mA}$	-500	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ mA}$, Referenced to 25°C	-	0.42	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
		$V_{DS} = -400\text{ V}, T_C = 125^\circ\text{C}$	-	-	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ mA}$	-3.0	-	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.05\text{ A}$	-	3.9	4.9	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.05\text{ A}$	-	2.1	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	510	660	pF
C_{oss}	Output Capacitance		-	70	90	pF
C_{rss}	Reverse Transfer Capacitance		-	9.5	12	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -250\text{ V}, I_D = -2.7\text{ A}, R_G = 25\ \Omega$ (Note 6)	-	12	35	ns
t_r	Turn-On Rise Time		-	56	120	ns
$t_{d(off)}$	Turn-Off Delay Time		-	35	80	ns
t_f	Turn-Off Fall Time		-	45	100	ns
Q_g	Total Gate Charge	$V_{DS} = -400\text{ V}, I_D = -2.7\text{ A}, V_{GS} = -10\text{ V}$ (Note 6)	-	18	23	nC
Q_{gs}	Gate-Source Charge		-	3.6	-	nC
Q_{gd}	Gate-Drain Charge		-	9.2	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–2.1	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	–8.4	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –2.1 A	–	–	–5.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = –2.7 A, dI _F / dt = 100 A/ms	–	270	–	ns
Q _{rr}	Reverse Recovery Charge		–	1.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CURVES

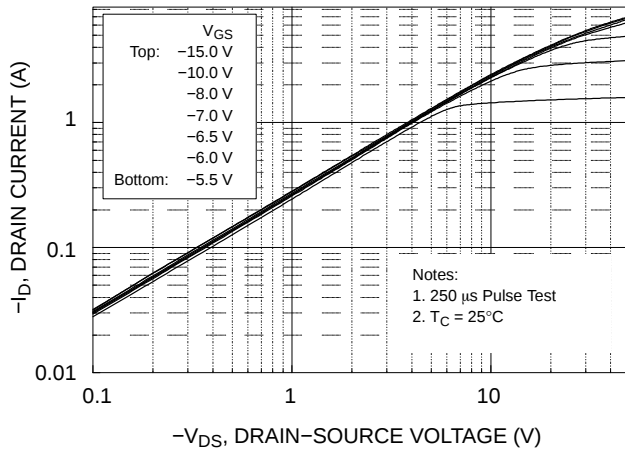


Figure 1. On-Region Characteristics

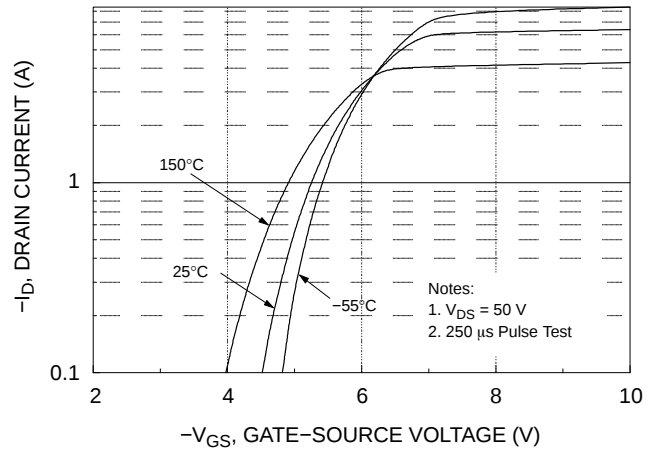


Figure 2. Transfer Characteristics

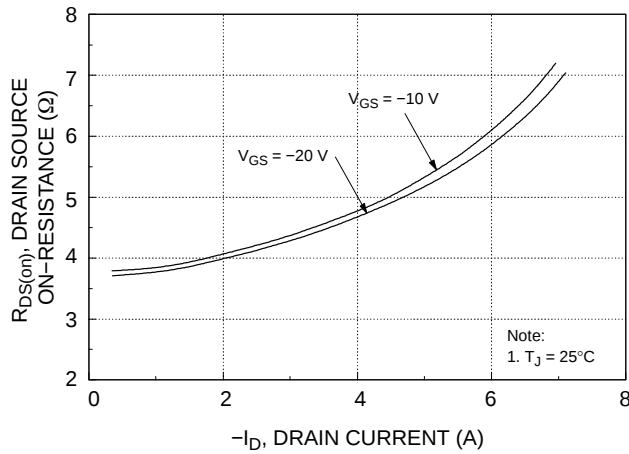


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

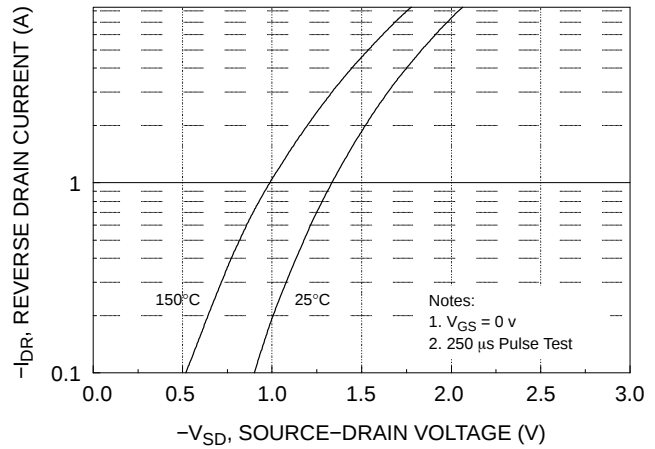


Figure 4. Body Diode Forward Voltage Variant vs. Source Current and Temperature

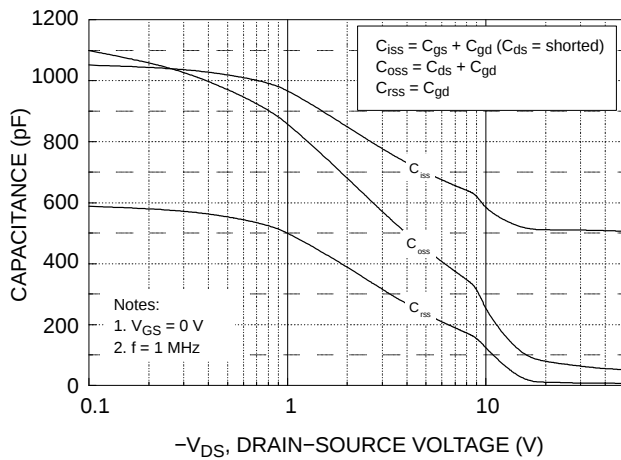


Figure 5. Capacitance Characteristics

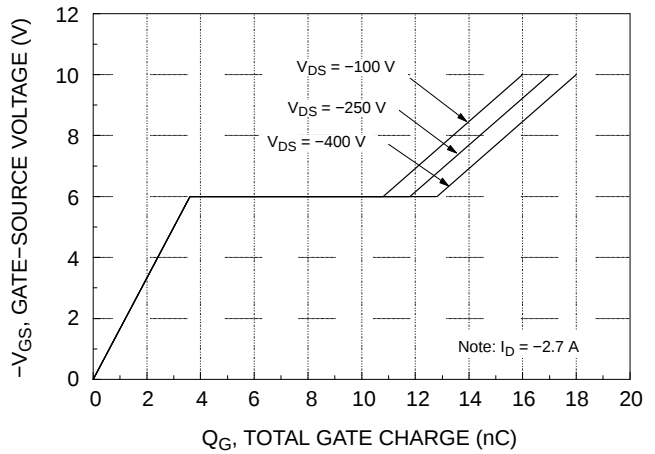


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CURVES (CONTINUED)

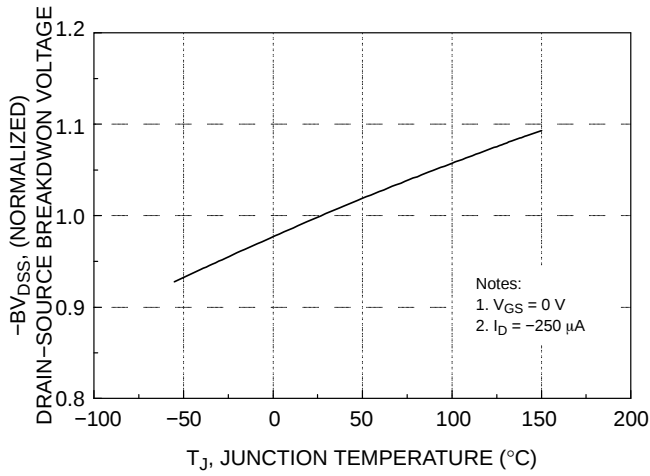


Figure 7. Breakdown Voltage Variation vs. Temperature

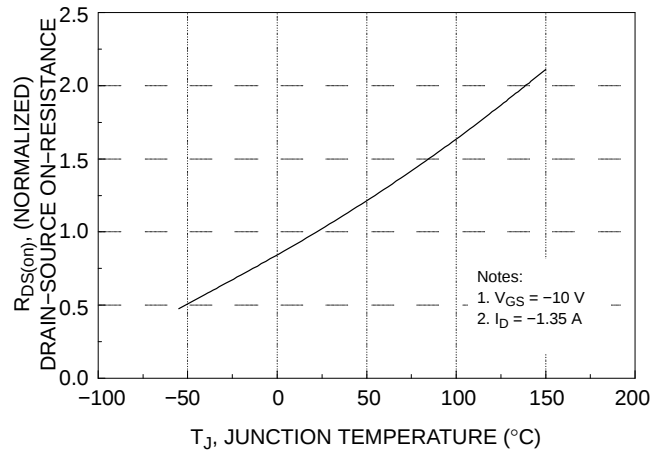


Figure 8. On-Resistance Variation vs. Temperature

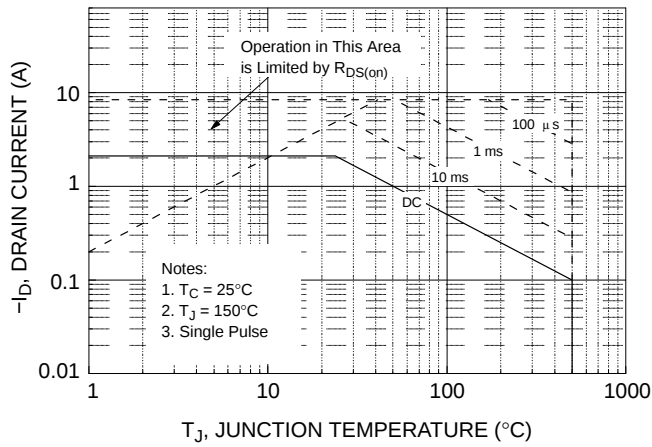


Figure 9. Maximum Safe Operation Area

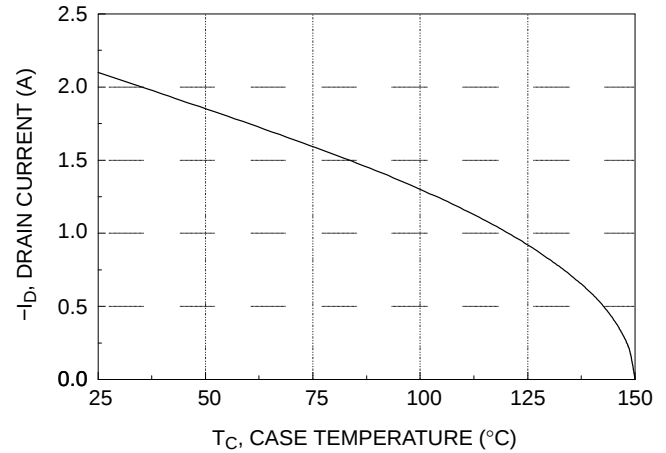


Figure 10. Maximum Drain Current vs. Case Temperature

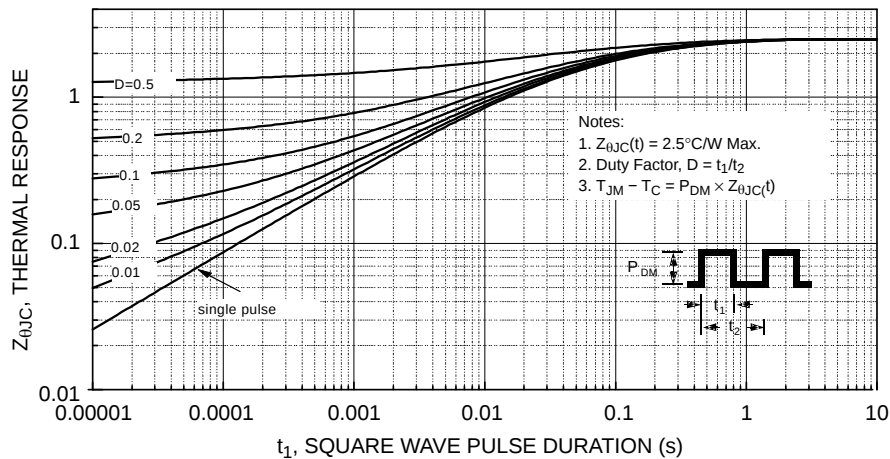


Figure 11. Transient Thermal Response Curve

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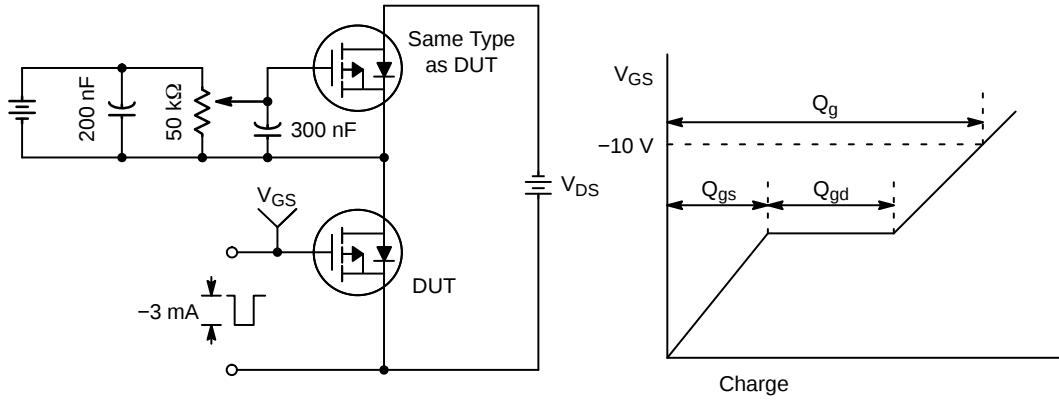


Figure 12. Gate Charge Test Circuit & Waveform

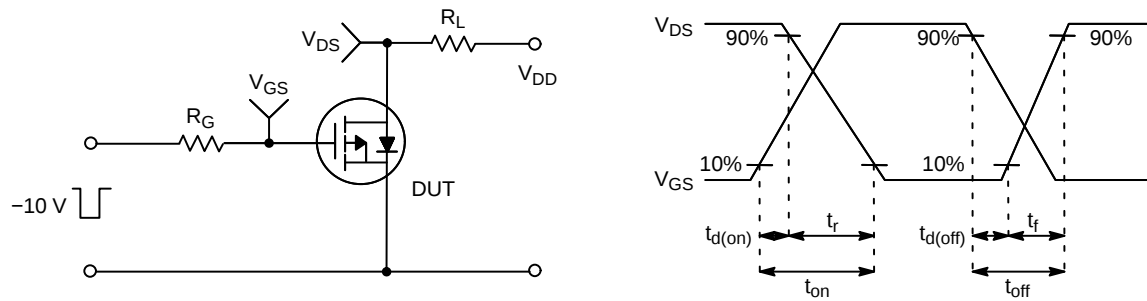


Figure 13. Resistive Switching Test Circuit & Waveforms

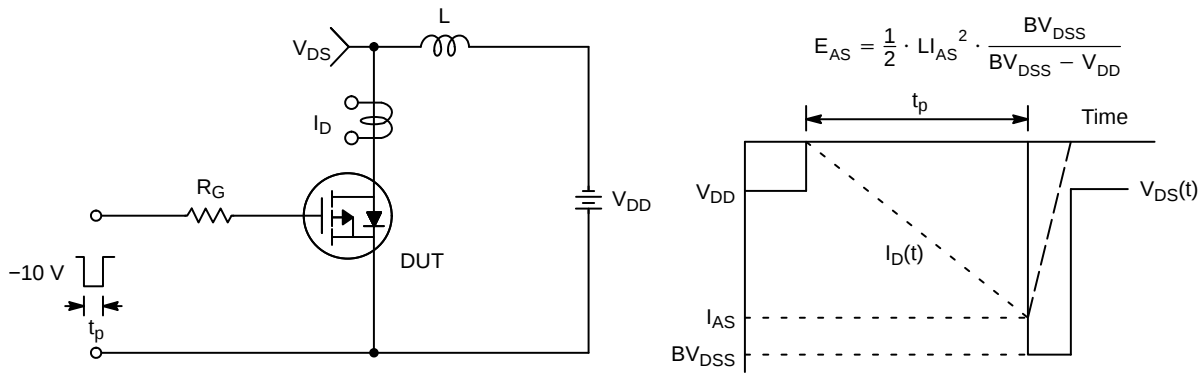


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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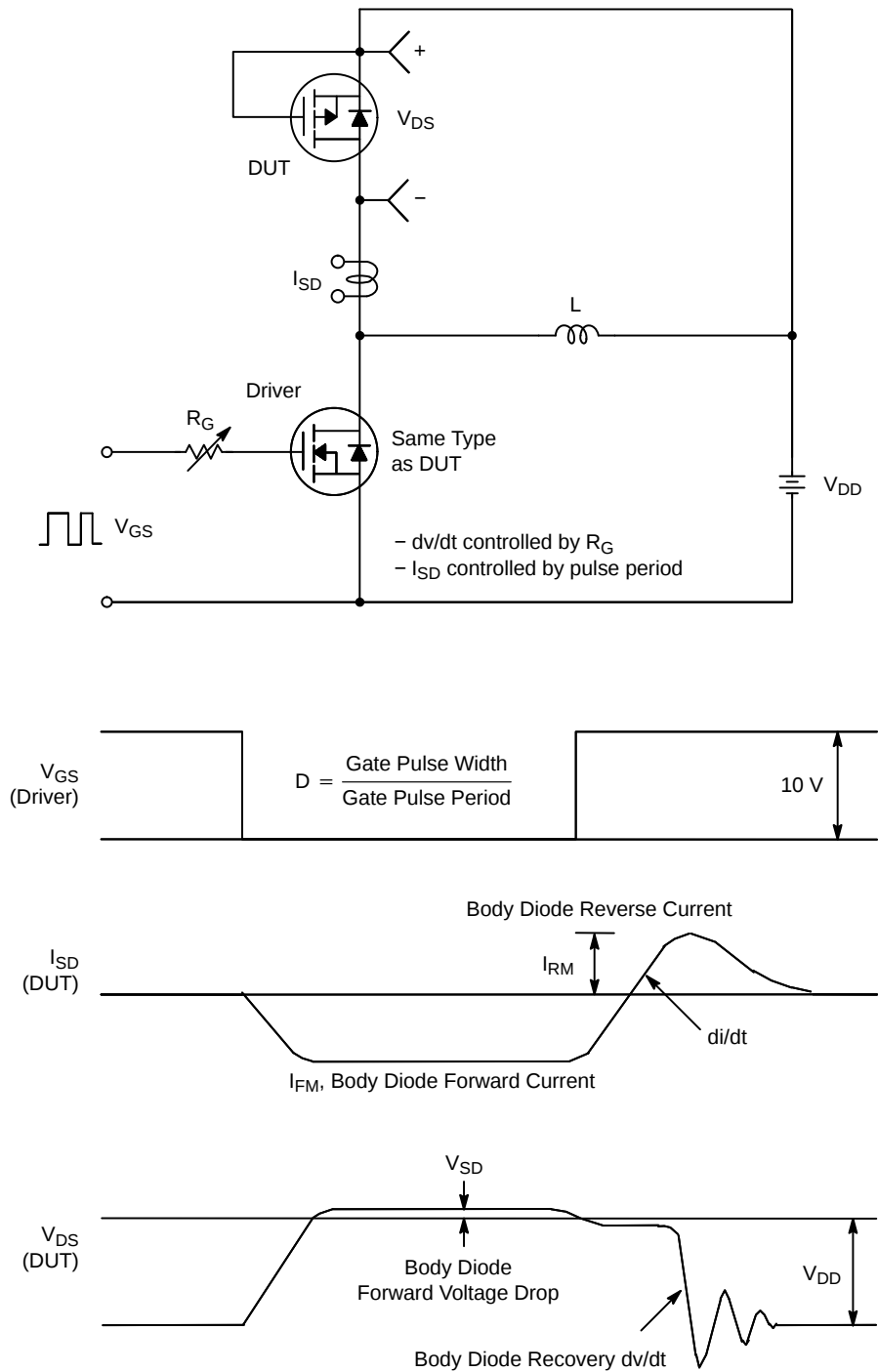


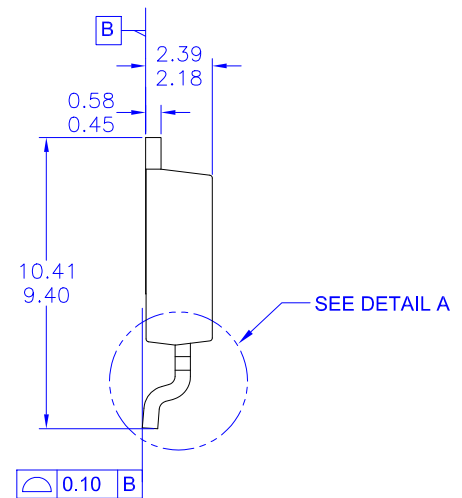
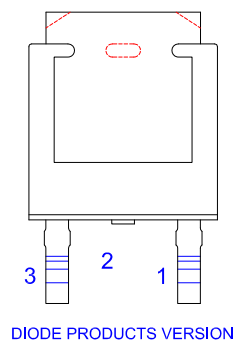
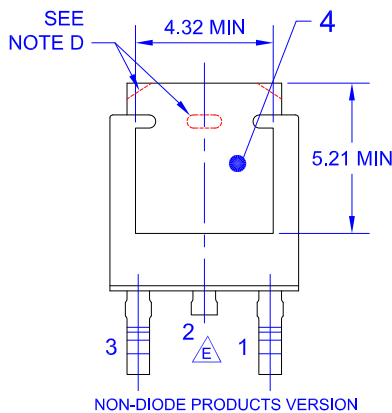
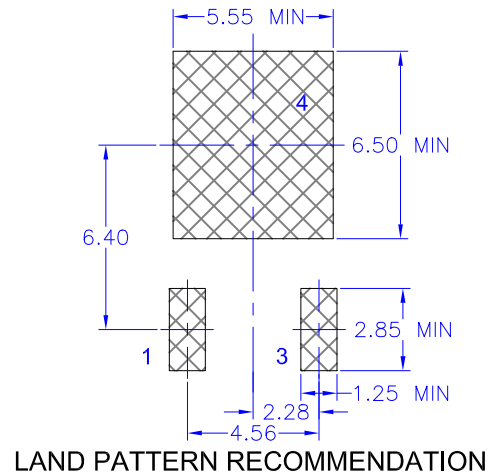
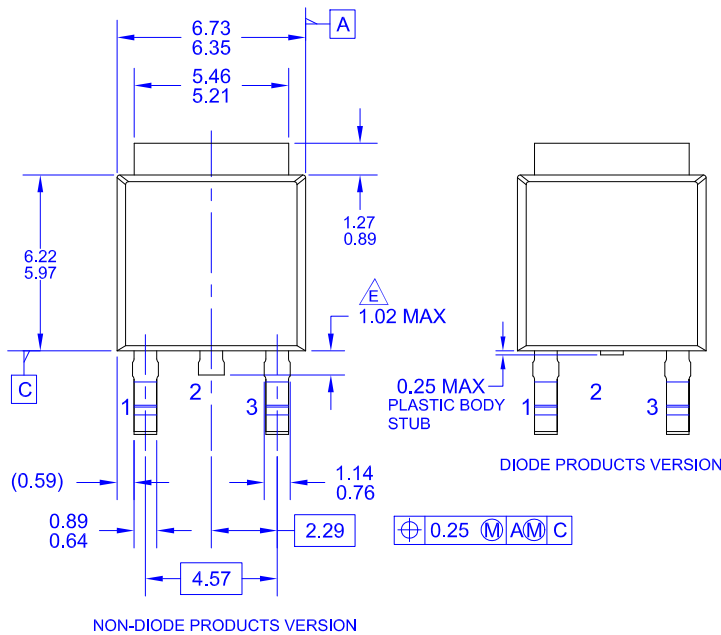
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DPAK3 (TO-252 3 LD)

CASE 369AS

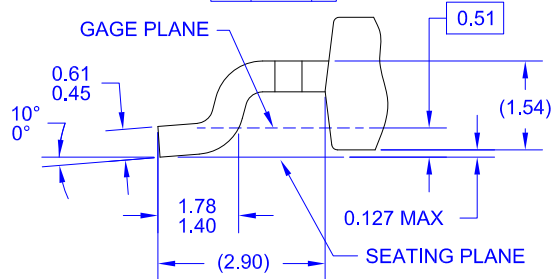
ISSUE O

DATE 30 SEP 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



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